

What Is Claimed Is:

1 1. A method of reducing an aspect ratio of a trench,
2 comprising the steps of:
3 forming a trench in a substrate;
4 forming a conformal first insulating layer on a surface of
5 the trench;
6 forming a conformal second insulating layer on the first
7 insulating layer;
8 forming a conformal third insulating layer on the second
9 insulating layer;
10 anisotropically etching the first, second and third
11 insulating layers to form a remaining first
12 insulating layer on a sidewall of the trench, a
13 remaining second insulating layer on the remaining
14 first insulating layer and a remaining third
15 insulating layer on the remaining second insulating
16 layer; and
17 performing an etching procedure with an etchant to remove
18 the remaining third insulating layer at a third
19 etching rate, part of the remaining second insulating
20 layer at a second etching rate and part of the
21 remaining first insulating layer at a first etching
22 rate;
23 wherein the third etching rate is greater than the second
24 etching rate and the second etching rate is greater
25 than the first etching rate.

1 2. The method according to claim 1, wherein the remaining
2 first insulating layer, the remaining second insulating layer
3 and the remaining third insulating layer are lower than a top
4 surface of the substrate.

1 3. A method of reducing an aspect ratio of a trench,
2 comprising the steps of:

3 forming a trench in a substrate;

4 using HDP-CVD to form a conformal Si-rich oxide layer on
5 a surface of the trench;

6 using HDP-CVD to form a conformal first oxide layer on the
7 Si-rich oxide layer;

8 using LP-CVD to form a conformal second oxide layer on the
9 first oxide layer;

10 anisotropically etching the Si-rich oxide layer, the first
11 oxide layer and the second oxide layer to form a
12 remaining Si-rich oxide layer on a sidewall of the
13 trench, a remaining first oxide layer on the
14 remaining Si-rich layer and a remaining second oxide
15 layer on the remaining first oxide layer; and

16 performing an etching procedure with an etchant to remove
17 the remaining second oxide layer at a third etching
18 rate, part of the remaining first oxide layer at a
19 second etching rate and part of the remaining Si-rich
20 oxide layer at a first etching rate;

21 wherein the third etching rate is greater than the second
22 etching rate and the second etching rate is greater
23 than the first etching rate.

1 4. The method according to claim 3, wherein the remaining
2 Si-rich oxide layer, the remaining first oxide layer and the
3 remaining second oxide layer are lower than a top surface of the
4 substrate.

1 5. The method according to claim 3, wherein the formation
2 of the trench comprises the steps of:
3 forming a shield layer on part of the substrate; and
4 using the shield layer as a mask, etching part of the
5 substrate to define the trench therein.

1 6. The method according to claim 5, wherein the shield
2 layer comprises a pad oxide layer and a silicon nitride layer.

1 7. The method according to claim 3, further comprising,
2 before forming the Si-rich layer, a step of:
3 forming a conformal linear layer on the surface of the
4 trench.

1 8. The method according to claim 3, wherein the first
2 oxide layer is a SiO₂ layer formed by HDP-CVD.

1 9. The method according to claim 3, wherein the second
2 oxide layer is a TEOS-SiO₂ layer formed by LP-CVD.

1 10. The method according to claim 3, wherein the etchant
2 is a BOE solution.

1 11. The method according to claim 10, wherein the third
2 etching rate is 800Å/min, the second etching rate is 400Å/min
3 and the first etching rate is 200Å/min.

1 12. The method according to claim 3, wherein a thickness
2 of the Si-rich layer is 50~100Å, a thickness of the first oxide
3 layer is 100~120Å and a thickness of the second oxide layer is
4 100~150Å.

1 13. A method of reducing an aspect ratio of a trench,
2 comprising the steps of:
3 forming a trench in a Si substrate;
4 using HDP-CVD, forming a conformal Si-rich oxide layer on
5 a surface of the trench, wherein a thickness of the
6 Si-rich layer is 50~100Å;
7 using HDP-CVD, forming a conformal first silicon oxide
8 layer on the Si-rich oxide layer, wherein a thickness
9 of the first oxide layer is 100~120Å;
10 using LP-CVD, forming a conformal second silicon oxide
11 layer on the first silicon oxide layer, wherein a
12 thickness of the second oxide layer is 100~150Å;
13 anisotropically etching the Si-rich oxide layer, the first
14 silicon oxide layer and the second silicon oxide
15 layer to form a remaining Si-rich oxide layer on a
16 sidewall of the trench, a remaining first silicon
17 oxide layer on the remaining Si-rich layer and a
18 remaining second silicon oxide layer on the remaining
19 first silicon oxide layer; and
20 performing an etching procedure with a BOE solution to
21 remove the remaining second silicon oxide layer at
22 a third etching rate, part of the remaining first
23 silicon oxide layer at a second etching rate and part

24 of the remaining Si-rich oxide layer at a first
25 etching rate;
26 wherein the third etching rate is greater than the second
27 etching rate and the second etching rate is greater
28 than the first etching rate.

1 14. The method according to claim 13, wherein the
2 remaining Si-rich oxide layer, the remaining first silicon oxide
3 layer and the remaining second silicon oxide layer are lower than
4 a top surface of the silicon substrate.

1 15. The method according to claim 13, wherein the
2 formation of the trench comprises the steps of:
3 forming a shield layer on part of the silicon substrate;
4 and
5 using the shield layer as a mask, etching part of the
6 silicon substrate to define the trench therein.

1 16. The method according to claim 15, wherein the shield
2 layer comprises a pad oxide layer and a silicon nitride layer.

1 17. The method according to claim 13, further comprising,
2 before forming the Si-rich layer, a step of:
3 forming a conformal linear layer on the surface of the
4 trench.

1 18. The method according to claim 13, wherein the first
2 silicon oxide layer is a SiO₂ layer formed by HDP-CVD.

1 19. The method according to claim 13, wherein the second
2 silicon oxide layer is a TEOS-SiO₂ layer formed by LP-CVD.

Client's ref.: NTC-91198/吳昌榮等
File: 0548-9346usf/Jacky/Steve

1 20. The method according to claim 13, wherein the third
2 etching rate is 800Å/min, the second etching rate is 400Å/min
3 and the first etching rate is 200Å/min.